

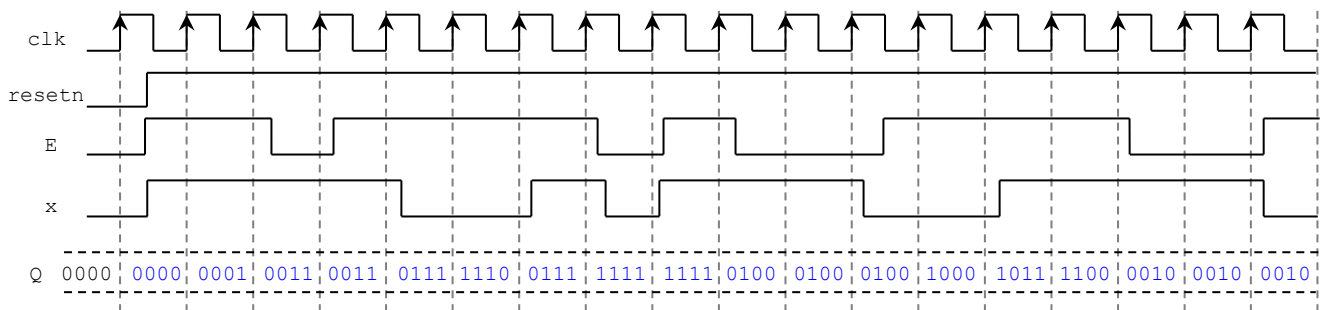
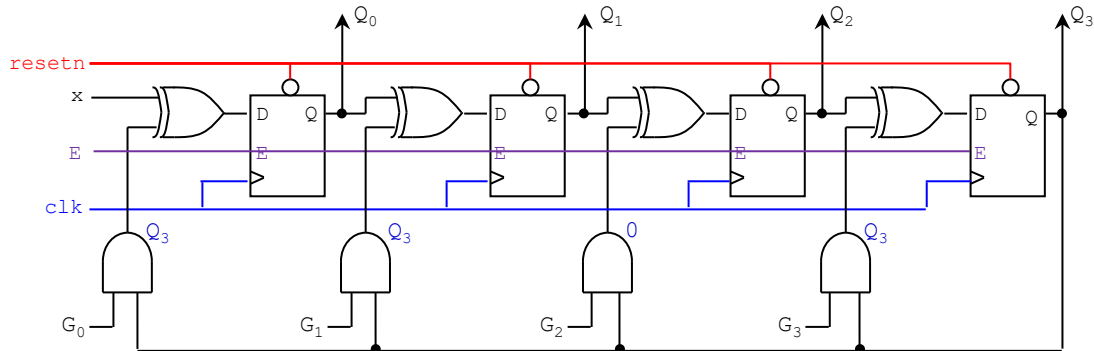
Solutions - Homework 4

(Due date: November 14th @ 11:59 pm)

Presentation and clarity are very important! Show your procedure!

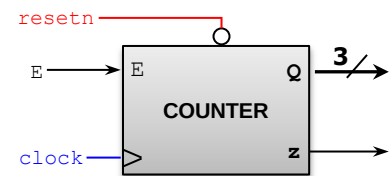
PROBLEM 1 (12 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1011$, $Q = Q_3Q_2Q_1Q_0$



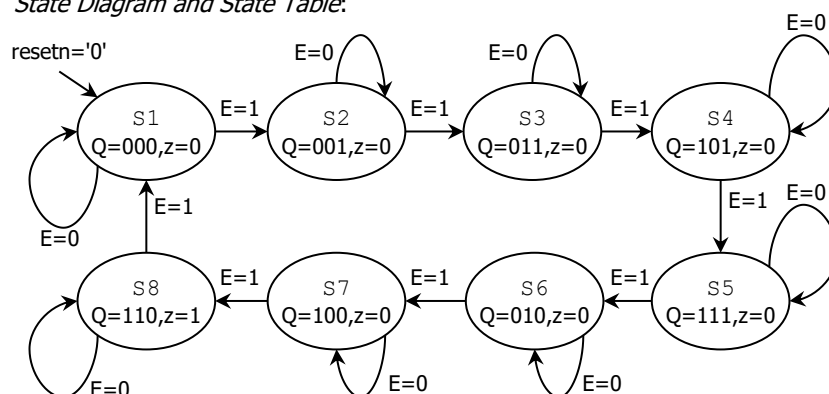
PROBLEM 2 (21 PTS)

- Design a counter using a Finite State Machine (FSM):
Counter features:
 - ✓ Count: 000, 001, 011, 101, 111, 010, 100, 110, 000, 001, 011, 101, ...
 - ✓ Input E: Synchronous input that increases the count when it is set to '1'.
 - ✓ Output z: It becomes '1' when the count is 110.
 - ✓ resetn: Asynchronous active-low input signal. It initializes the count to 000.



- Provide the State Diagram (any representation), State Table, and the Excitation Table of this circuit. (13 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. Is this a Mealy or a Moore machine? Why? (3 pts)

- State Diagram and State Table:

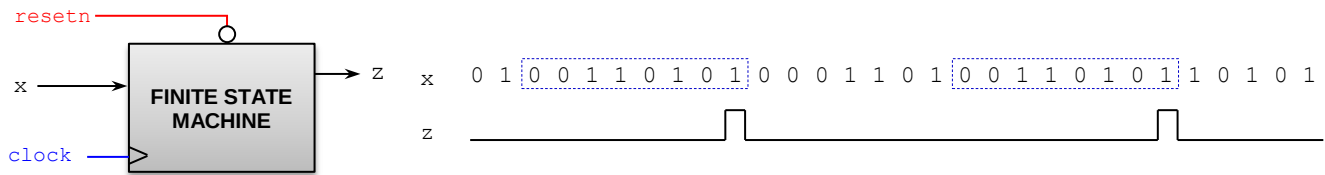


The output z only depends on the present state $\Rightarrow$ Moore FSM.

PRESENT		NEXT	
E	STATE	STATE	z
0	S1	S1	0
0	S2	S2	0
0	S3	S3	0
0	S4	S4	0
0	S5	S5	0
0	S6	S6	0
0	S7	S7	0
0	S8	S8	1
1	S1	S2	0
1	S2	S3	0
1	S3	S4	0
1	S4	S5	0
1	S5	S6	0
1	S6	S7	0
1	S7	S8	0
1	S8	S1	1

PROBLEM 3 (20 PTS)

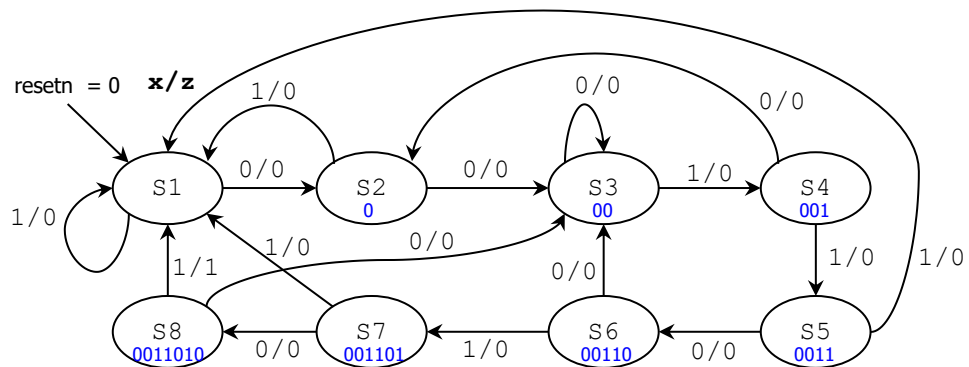
- Sequence detector: The machine generates $z = 1$ when it detects the sequence 00110101. Once the sequence is detected, the circuit looks for a new sequence.



- ✓ Draw the State Diagram (any representation) of this circuit with input x and output z . (5 pts)
- ✓ Complete the State Table and the Excitation Table. (4 pts)
- ✓ Which type is this FSM? (Mealy) (Moore) Why? _____

State Assignment:

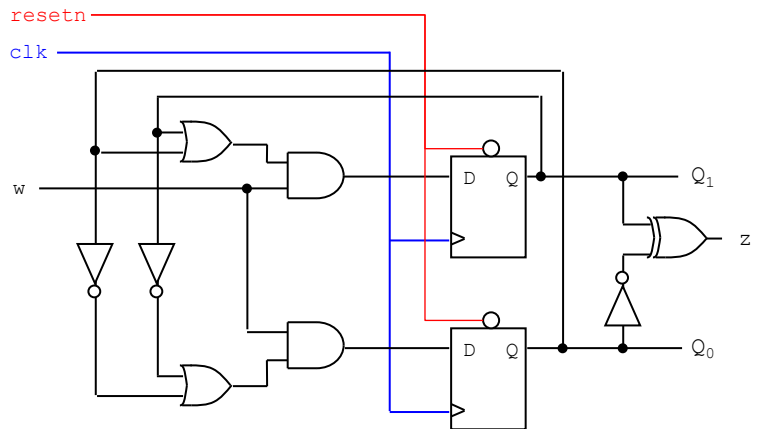
- S1: $Q = 000$
- S2: $Q = 001$
- S3: $Q = 010$
- S4: $Q = 011$
- S5: $Q = 100$
- S6: $Q = 101$
- S7: $Q = 110$
- S8: $Q = 111$



PRESENT STATE				NEXT STATE			
x	STATE	NEXT STATE	z	x	Q ₂ Q ₁ Q ₀ (t)	Q ₂ Q ₁ Q ₀ (t+1)	z
0	S1	S2	0	0	0 0 0	0 0 1	0
0	S2	S3	0	0	0 0 1	0 1 0	0
0	S3	S3	0	0	0 1 0	0 1 0	0
0	S4	S2	0	0	0 1 1	0 0 1	0
0	S5	S6	0	0	1 0 0	1 0 1	0
0	S6	S3	0	0	1 0 1	0 1 0	0
0	S7	S8	0	0	1 1 0	1 1 1	0
0	S8	S3	0	0	1 1 1	0 1 0	0
1	S1	S1	0	1	0 0 0	0 0 0	0
1	S2	S1	0	1	0 0 1	0 0 0	0
1	S3	S4	0	1	0 1 0	0 1 1	0
1	S4	S5	0	1	0 1 1	1 0 0	0
1	S5	S1	0	1	1 0 0	0 0 0	0
1	S6	S7	0	1	1 0 1	1 1 0	0
1	S7	S1	0	1	1 1 0	0 0 0	0
1	S8	S1	1	1	1 1 1	0 0 0	1

This is a Mealy FSM. The output z depends on the input as well as the present state.

- Given the following FSM circuit. (w : input, z : output, Q_1Q_0 : state) (10 pts)
 - ✓ Provide the Excitation Table, State Table, and the State Diagram (any representation).
 - ✓ Get the excitation equations and the Boolean equation for z . (6 pts)
 - ✓ Which type is this FSM? (1 pt.)
(Mealy) (Moore)



$$Q_1(t+1) \leftarrow (Q_1 + Q_0)w$$

$$Q_0(t+1) \leftarrow \overline{Q_1}Q_0w$$

$$z = \overline{Q_1} \oplus Q_0$$

State Assignment:

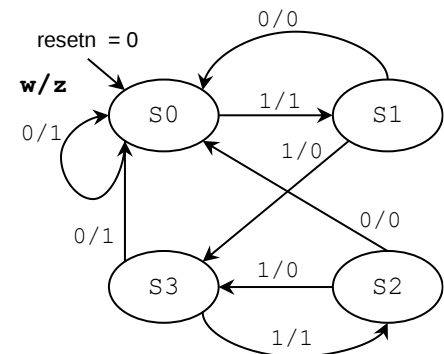
S0: $Q = 00$ S1: $Q = 01$

S2: $Q = 10$ S3: $Q = 11$

PRESENT STATE			NEXTSTATE		
w	$Q_1Q_0(t)$		$Q_1Q_0(t+1)$	z	
0	0 0	0	0 0	1	
0	0 1	0	0 0	0	
0	1 0	0	0 0	0	
0	1 1	0	0 0	1	
1	0 0	0	0 1	1	
1	0 1	1	1 1	0	
1	1 0	1	1 1	0	
1	1 1	1	1 0	1	



w	PRESENT STATE	NEXT STATE	z
0	S0	S0	1
0	S1	S0	0
0	S2	S0	0
0	S3	S0	1
1	S0	S1	1
1	S1	S3	0
1	S2	S3	0
1	S3	S2	1



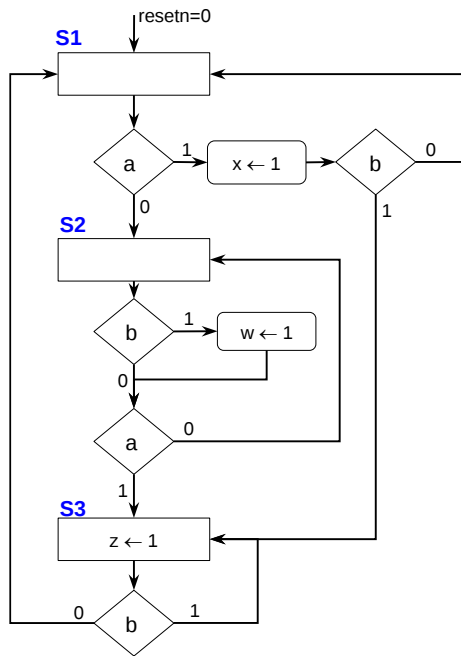
This is a Moore FSM. The output z depends only on the present state.

PROBLEM 4 (15 PTS)

- Provide the state diagram (in ASM form) of the FSM whose VHDL description is shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram. (9 pts)

```
library ieee;
use ieee.std_logic_1164.all;

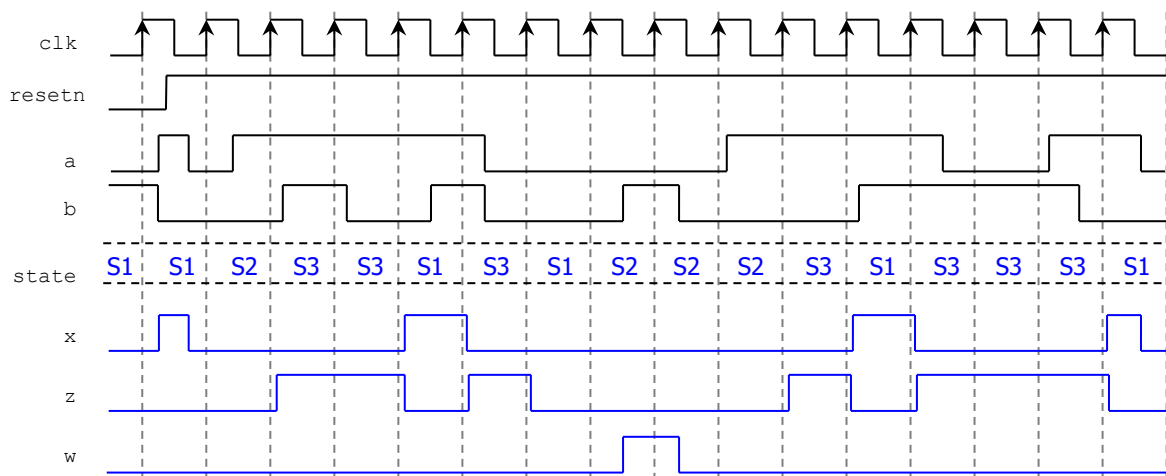
entity myfsm is
    port ( clk, resetn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end myfsm;
```



```
architecture behavioral of myfsm is
    type state is (S1, S2, S3);
    signal y: state;
begin
    Transitions: process (resetn, clk, a, b)
    begin
        if resetn = '0' then y <= S1;
        elsif (clk'event and clk = '1') then
            case y is
                when S1 =>
                    if a = '1' then
                        if b = '1' then y <= S3; else y <= S1; end if;
                    else
                        y <= S2;
                    end if;
                when S2 =>
                    if a = '1' then y <= S3; else y <= S2; end if;
                when S3 =>
                    if b = '1' then y <= S3; else y <= S1; end if;
            end case;
        end if;
    end process;

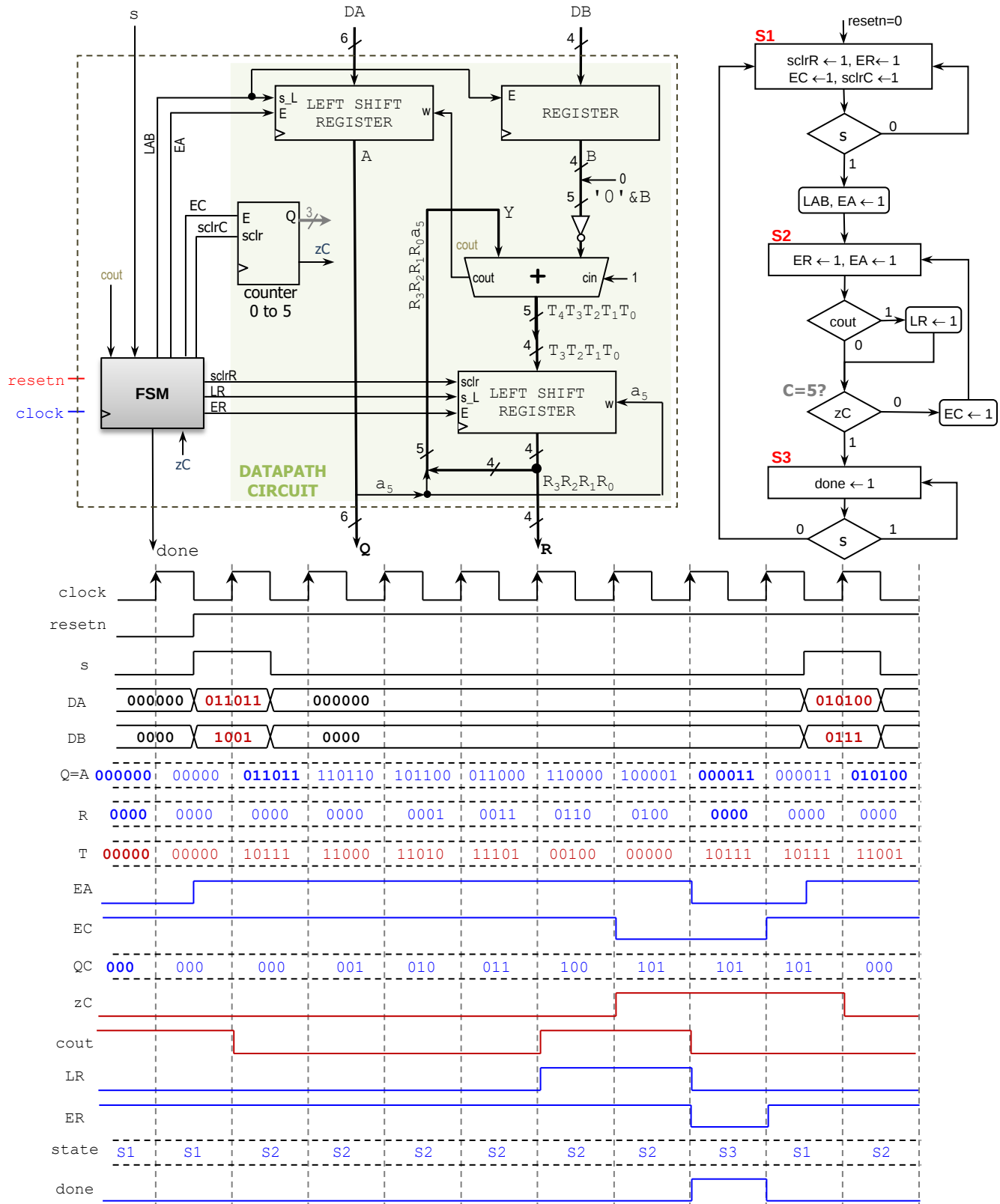
    Outputs: process (y, a, b)
    begin
        x <= '0'; w <= '0'; z <= '0';
        case y is
            when S1 => if a = '1' then x <= '1'; end if;
            when S2 => if b = '1' then w <= '1'; end if;
            when S3 => z <= '1';
        end case;
    end process;
end behavioral;
```

This is a Mealy FSM. The outputs depend on the input as well as the present state.



PROBLEM 5 (18 PTS)

- Complete the timing diagram of the following digital system that includes an FSM (in ASM form) and a datapath circuit. Generic components: counter, parallel access shift registers, register. See *Lecture Notes – Unit 6* for their behavior.



PROBLEM 6 (14 PTS)

- Attach a printout of your Project Status Report (no more than 3 pages, single-spaced, 2 columns). This report should contain the current status of the project, including more details about the design and its components. You **MUST** use the provided template (Final Project - Report Template.docx).